AMENDMENTS TO THE CLAIMS

Please cancel claims 13-25 without prejudice or disclaimer of their underlying subject matter.

1-25. (Canceled)

Please add the following new claims.

26. (New) A data processing apparatus comprising:

program memory adapted to store instruction codes as a program, a program address indicating a location within said program memory for one of the instruction codes;

a bug address setting register adapted to store a bug address, said bug address indicating a starting address within said program memory for a buggy part of said program; and

a counter register adapted to store a value, said value representing a number of times an interrupt request signal indicates a coincidence between said program address and said bug address.

27. (New) A data processing apparatus as set forth in claim 26, further comprising:

a coincidence detecting circuit adapted to compare said program address with said bug address and output said interrupt request signal,

wherein said interrupt request signal indicates coincidence or non-coincidence of said program address and said bug address.

28. (New) A data processing apparatus as set forth in claim 27, wherein said value is incremented when said interrupt request signal indicates said coincidence.

29. (New) A data processing apparatus as set forth in claim 26, further comprising:

a central processing unit adapted to receive said interrupt request signal.

30. (New) A data processing apparatus as set forth in claim 29, wherein said central processing unit reads an abort vector from said program memory when said interrupt request signal indicates said coincidence,

said abort vector indicating a starting address for a debugged program.

31. (New) A data processing apparatus as set forth in claim 30, wherein said abort vector is located within said random access memory.

32. (New) A data processing apparatus as set forth in claim 29, wherein said central processing unit receives said interrupt request signal.

33. (New) A data processing apparatus as set forth in claim 29, wherein said central processing unit reads said instruction codes sequentially from said program memory.

34. (New) A data processing apparatus as set forth in claim 29, wherein another program address indicates a location within said program memory for another of the instruction codes.

35. (New) A data processing apparatus as set forth in claim 34, further comprising:

another bug address setting register adapted to store another bug address, said another bug address indicating another starting address within said program memory for another buggy part of said program.

36. (New) A data processing apparatus as set forth in claim 35, wherein said value is incremented when another interrupt request signal indicates another coincidence between said program address and said another bug address.

37. (New) A data processing apparatus as set forth in claim 34, wherein said central processing unit is adapted use said value to select for correction said buggy part or said another buggy part.

38. (New) A data processing apparatus as set forth in claim 34, further comprising:

another coincidence detecting circuit adapted to compare said another program address with said another bug address and output another interrupt request signal,

wherein said another interrupt request signal indicates coincidence or non-coincidence of said another program address and said another bug address.

39. (New) A data processing apparatus as set forth in claim 34, wherein said counter register is located within said random access memory at a predetermined memory address.

40. (New) A data processing apparatus as set forth in claim 34, wherein said value of the counter register is incremented by 1.

41. (New) A data processing apparatus as set forth in claim 34, wherein debugged programs are stored within a random access memory.

42. (New) A data processing apparatus as set forth in claim 41, wherein said debugged programs stored within said random access memory is read from an external memory.

43. (New) A data processing apparatus as set forth in claim 41, wherein said debugged programs are stored within said random access memory during initialization processing.

44. (New) A data processing apparatus as set forth in claim 43, wherein said counter register is cleared during said initialization processing.